

Fig. 1

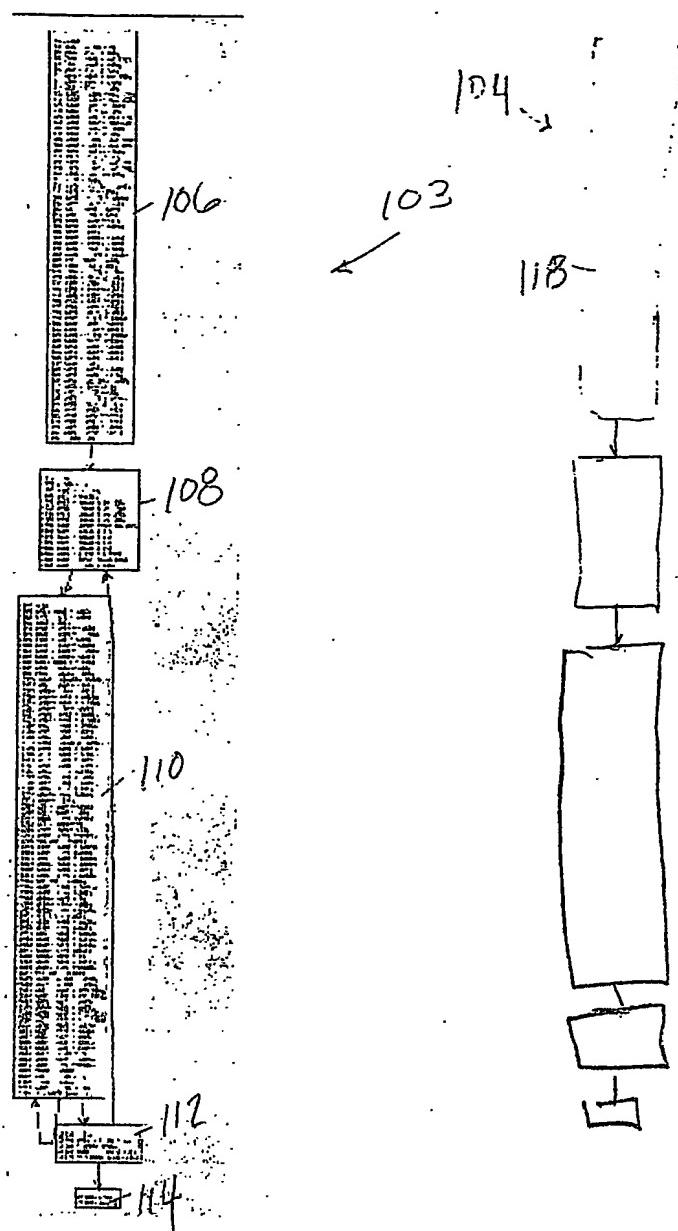


Fig. 2

(1)	1.25 = $\pi \cdot 173 / 71$
(2)	1.249 = $2 + 10.152$
(3)	1.248 = $1.249 - 0.001.1721$
(4)	1.247 = $1.248 - 1.1753$
(5)	1.246 = $1.247 - 1.1751$
(6)	1.245 = $1.246 - 0.001.1731$
(7)	1.244 = $1.245 - 1.1735$
(8)	1.243 = $1.244 - 1.1731$
(9)	1.242 = $1.243 - 1.1735$
(10)	1.241 = $1.242 - 1.1731$
(11)	1.240 = $1.241 - 1.1731$
(12)	1.239 = $1.240 - 1.1731$
(13)	1.238 = $2 + 1.1731$
(14)	1.237 = $1.238 - 1.1731$
(15)	1.236 = $1.237 - 0.001.1731$
(16)	1.235 = $1.236 - 1.1731$
(17)	1.234 = $1.235 - 1.1731$
(18)	1.233 = $1.234 - 1.1731$
(19)	1.232 = $1.233 - 1.1731$
(20)	1.231 = $1.232 - 1.1731$
(21)	1.230 = $1.231 - 1.1731$
(22)	1.229 = $1.230 - 1.1731$
(23)	1.228 = $1.229 - 1.1731$
(24)	1.227 = $1.228 - 1.1731$
(25)	1.226 = 281
(26)	1.225 = $40.168 - 1.2421$
(27)	1.224 = $16 - 1.1731$
(28)	1.223 = $r.173 - 1.2309$
(29)	1.222 = $10 - 1.169$
(30)	1.221 = $1.222 - 1.1641$
(31)	1.220 = $-80 - 1.123$
(32)	1.219 = $1.220 - 1.1231$
(33)	1.218 = $1.219 - 1.1231$
(34)	1.217 = $1.218 - 1.1231$
(35)	1.216 = $1.217 - 1.1231$
(36)	1.215 = $1.216 - 1.1231$
(37)	1.214 = $1.215 - 1.1231$
(38)	1.213 = $1.214 - 1.1231$
(39)	1.212 = $1.213 - 1.1231$
(40)	1.211 = $1.212 - 1.1231$
(41)	1.210 = $1.211 - 1.1231$
(42)	1.209 = $16 - 1.1231$
(43)	1.208 = $1.209 - 1.1231$
(44)	1.207 = $1.208 - 1.1231$
(45)	1.206 = $1.207 - 1.1231$
(46)	1.205 = $1.206 - 1.1231$
(47)	1.204 = $1.205 - 1.1231$
(48)	1.203 = $1.204 - 1.1231$
(49)	1.202 = $r.173 - 1.2309$
(50)	1.201 = $1.202 - 1.1231$
(51)	1.200 = $-12 - 1.1231$
(52)	1.199 = $r.173 - 1.2309$
(53)	1.198 = $16 - 1.1721$
(54)	1.197 = $1.198 - 1.1665$
(55)	1.196 = $1.197 - 1.1665$
(56)	1.195 = $1.196 - 1.1665$
(57)	1.194 = 244
(58)	1.193 = $1.194 - 1.1665$
(59)	1.192 = $1.193 - 1.1665$
(60)	1.191 = $1.192 - 1.1665$
(61)	1.190 = $10.167 - 1.1549$
(62)	1.189 = $15 - 1.1415$
(63)	1.188 = $1.189 - 1.1223$
(64)	1.187 = $r.173 - 1.1334$
(65)	1.186 = $10 - 12.1711$
(66)	1.185 = $1.186 - 1.1273$
(67)	1.184 = $1.185 - 1.1273$
(68)	1.183 = $1.184 - 1.1273$
(69)	1.182 = $1.183 - 1.1273$
(70)	1.181 = $1.182 - 1.1273$
(71)	1.180 = $1.181 - 1.1273$

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Fig. 3

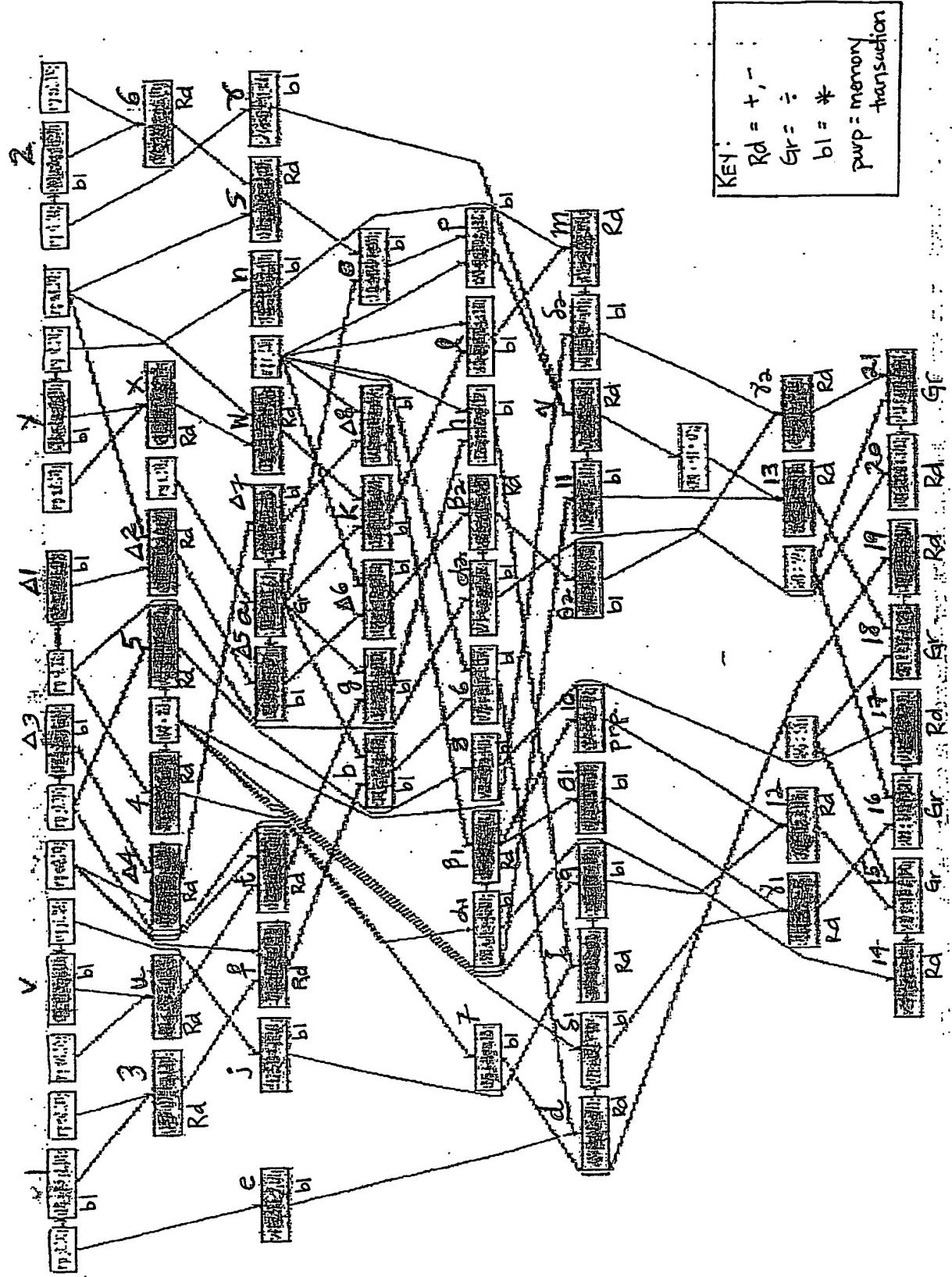


Fig. 4(a)

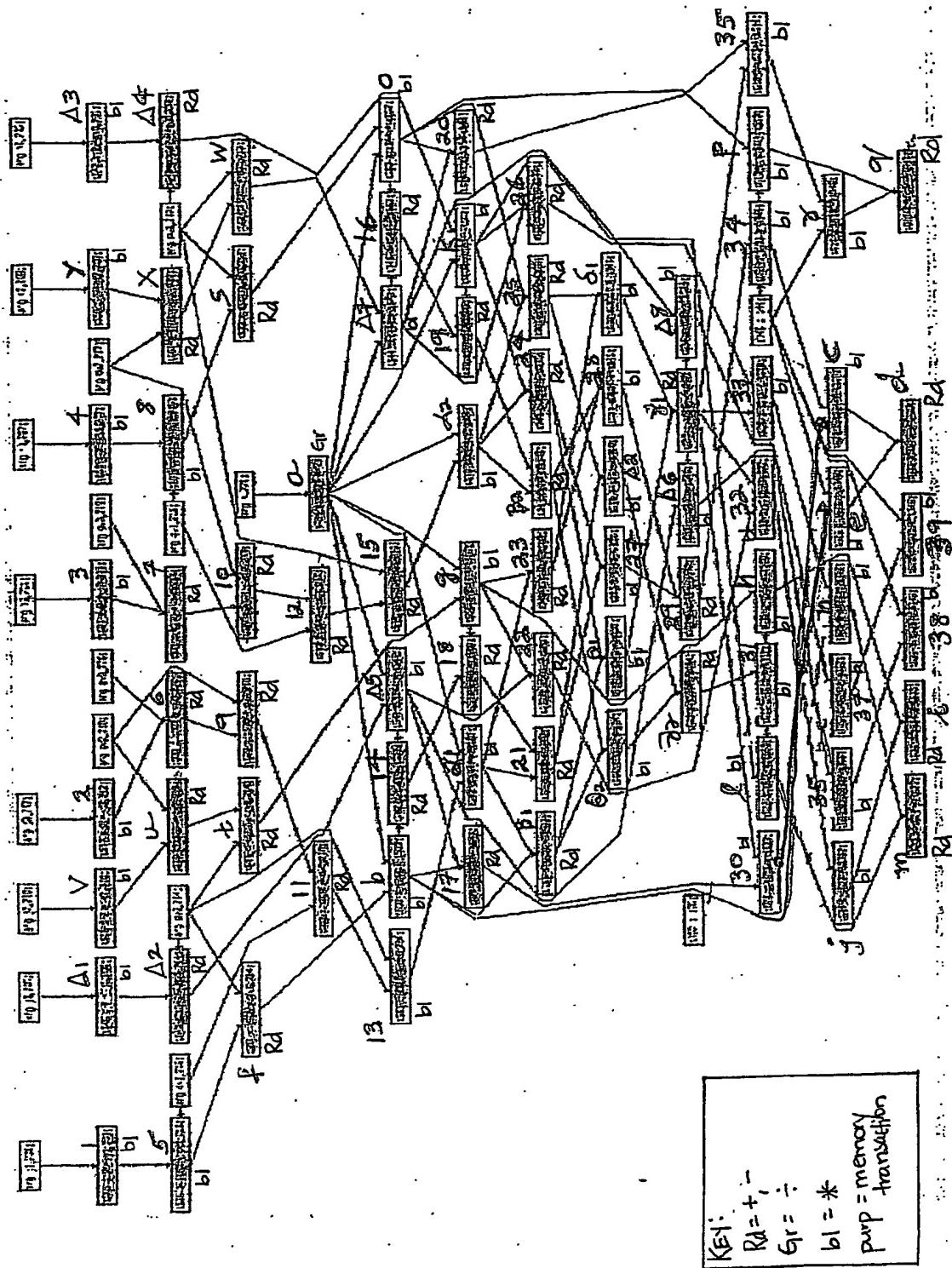


Fig. 4(b)

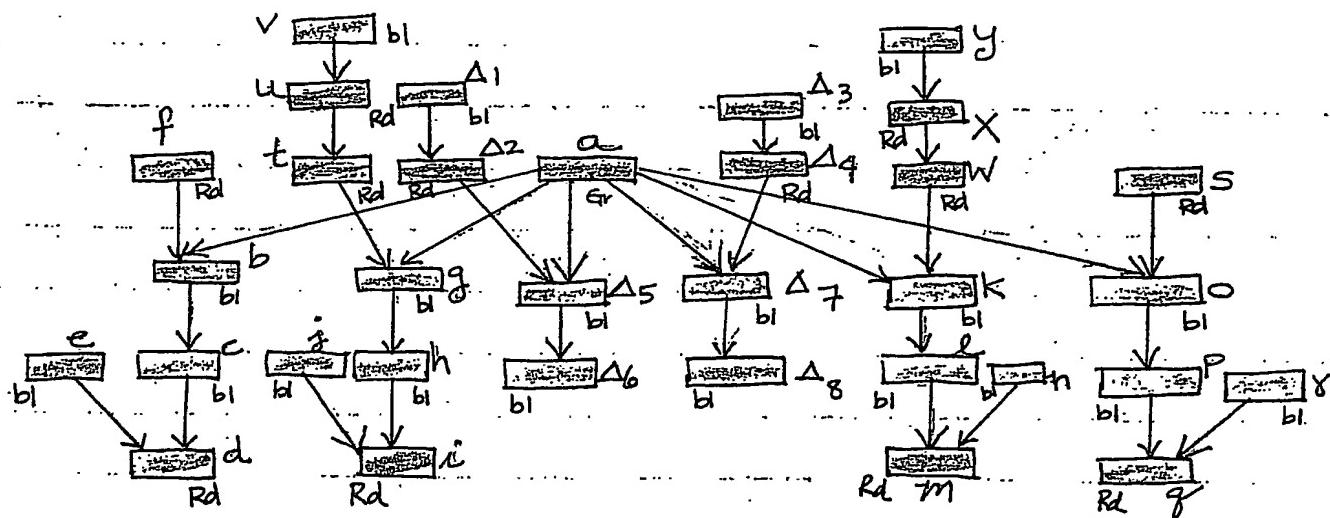
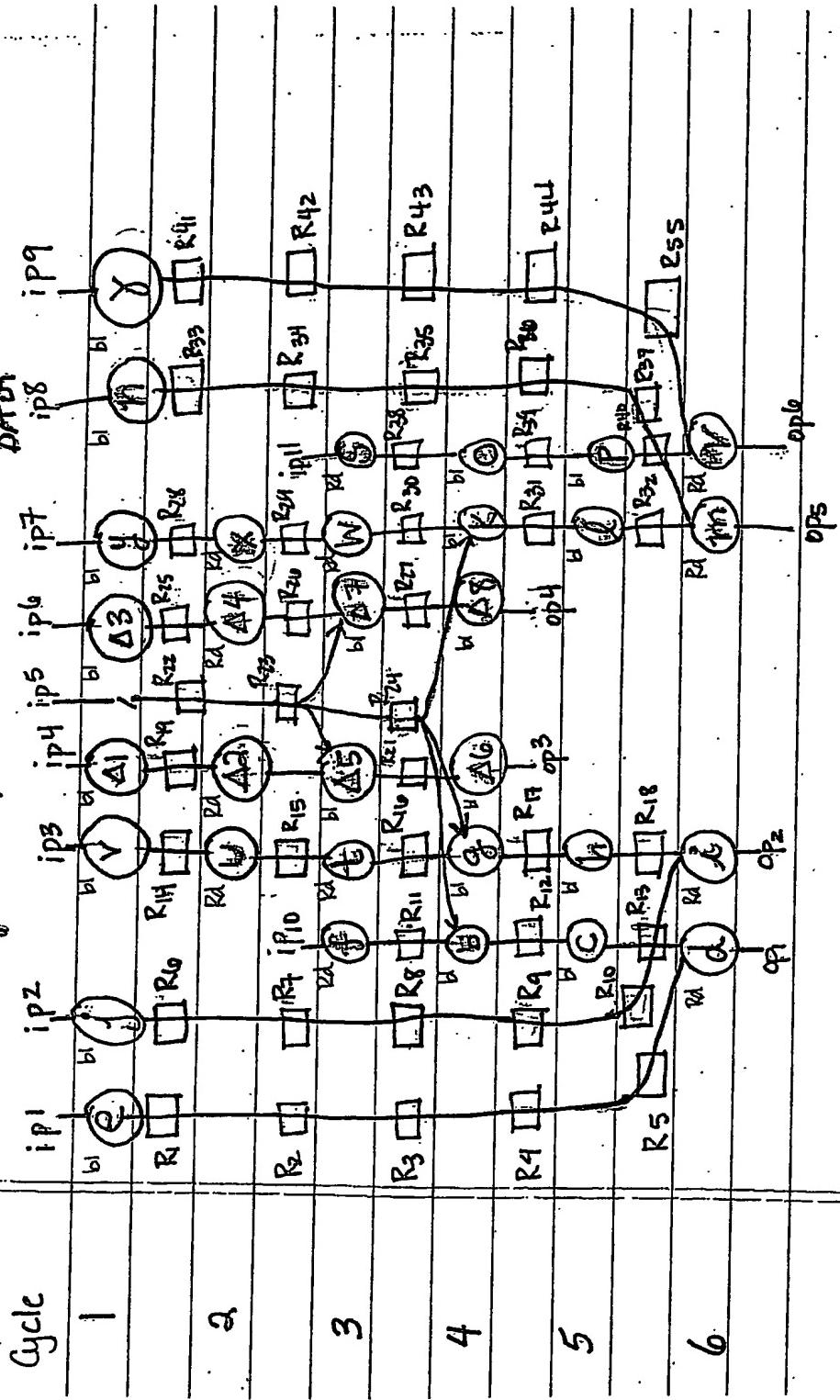


Fig. 5

KEY:
 $Rd = +, -$
 $Gr = \div$
 $bl = *$
 pup = memory transaction

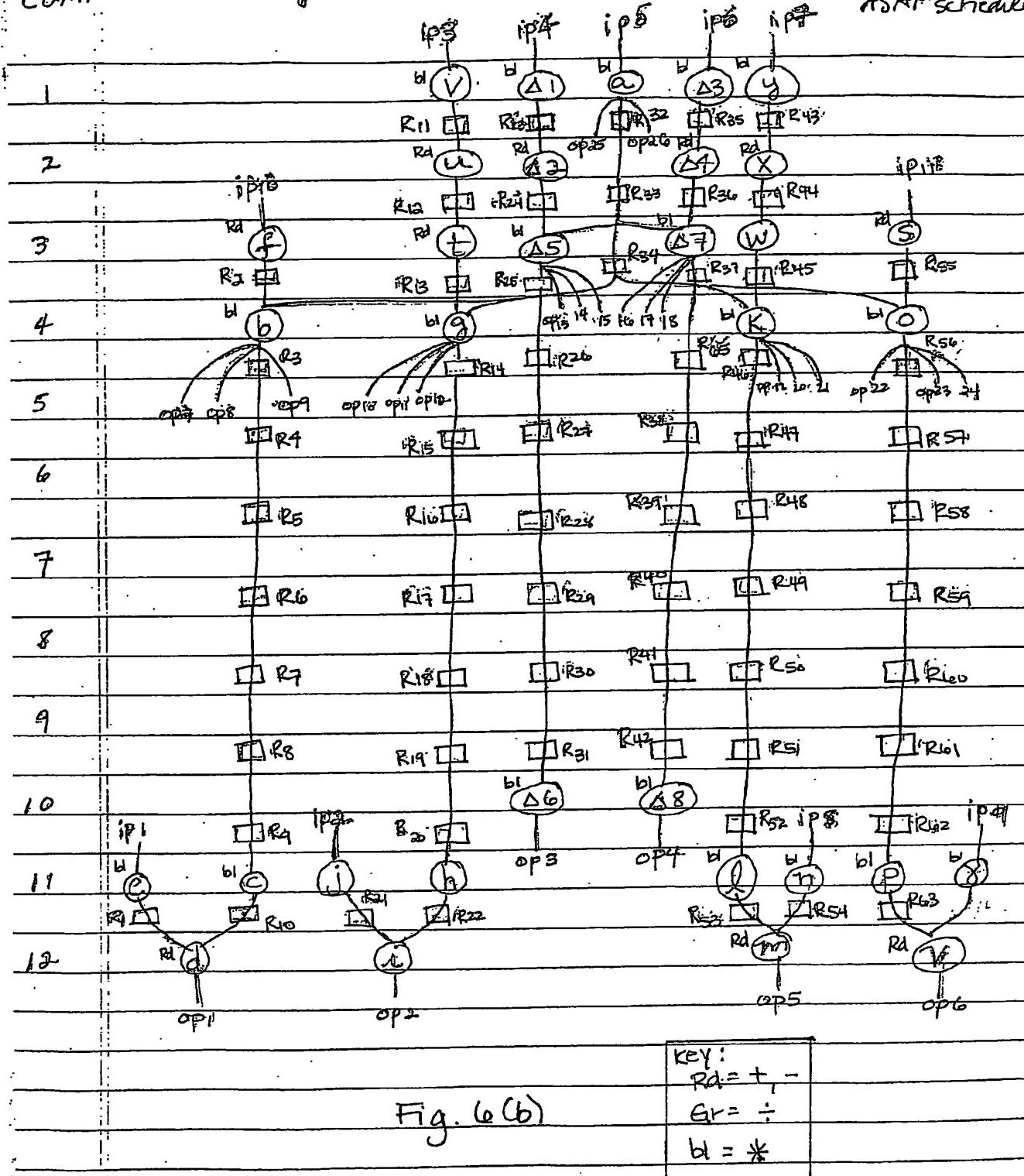
Common L-L mapping of Example mapped onto Affine with ASAPS schedule



Key:
$Rd = +,-$
$Gr = \div$
$bl = *$

Fig. 6(a)

Common LCS-G of Example mapped onto Perspective DAG with ASAP schedule



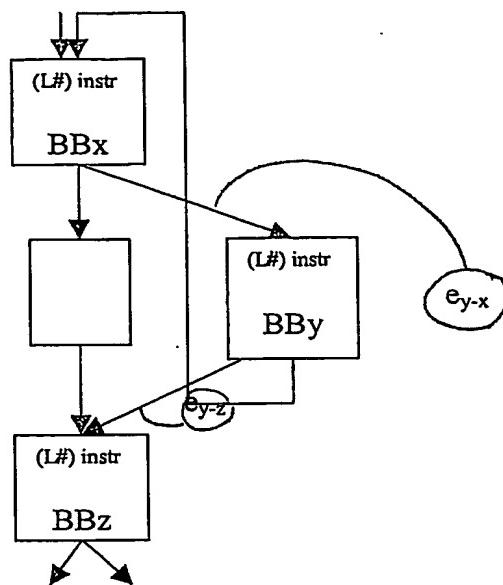


Fig. 7

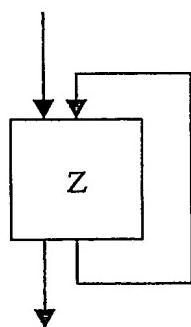


Fig. 8

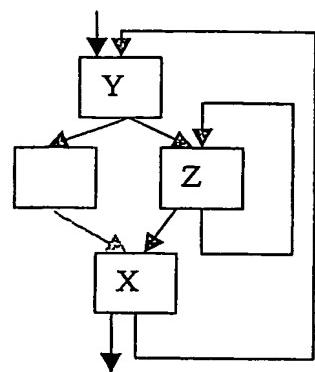


Fig. 9 (a)

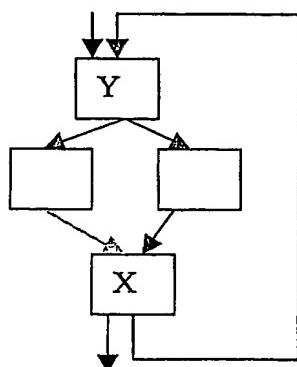


Fig. 9 (b)

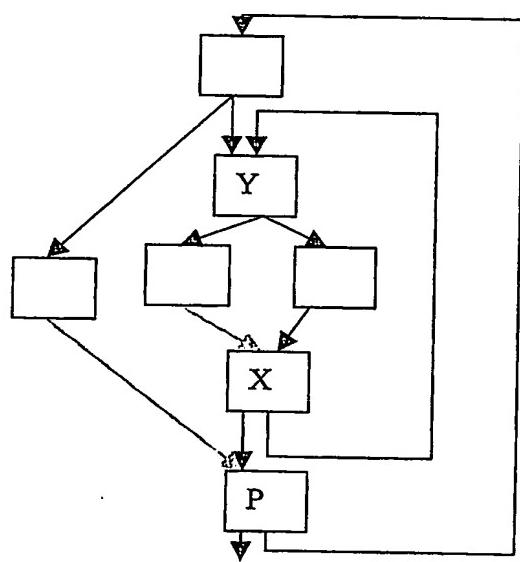


Fig. 10

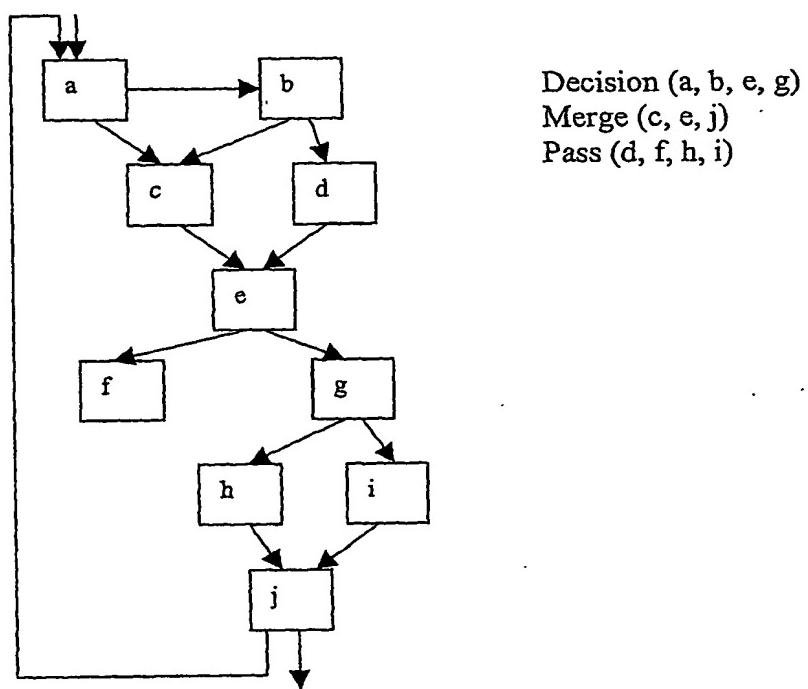


Fig. 11

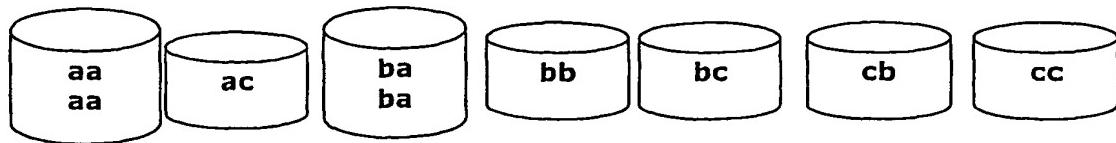
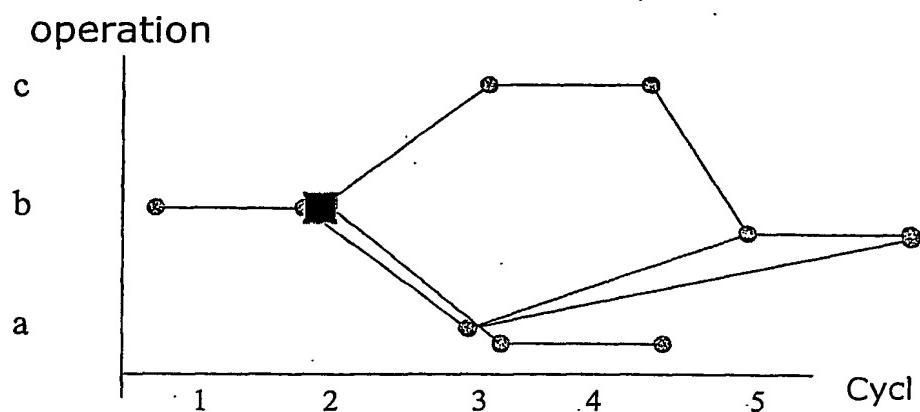
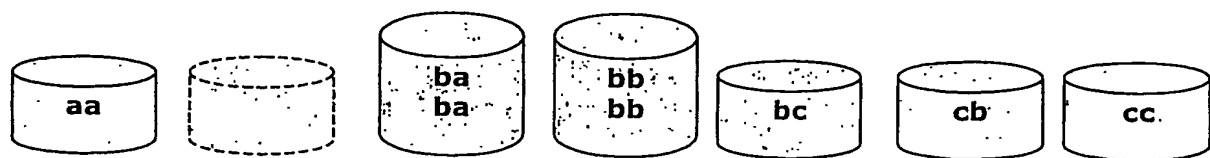


Figure 12: First Graph's edges arranged into a Bin Sequence



Graph number 2, Figure 13: The Second Graph



13(c)
Figure 14: The Second Graph arranged in a Modified Bin Sequence

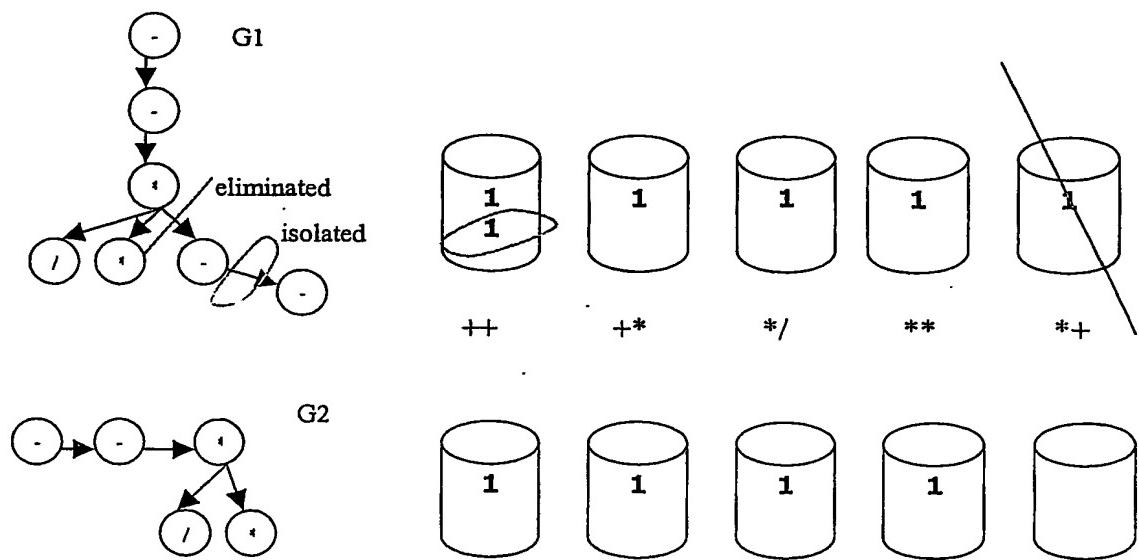


Fig. 14

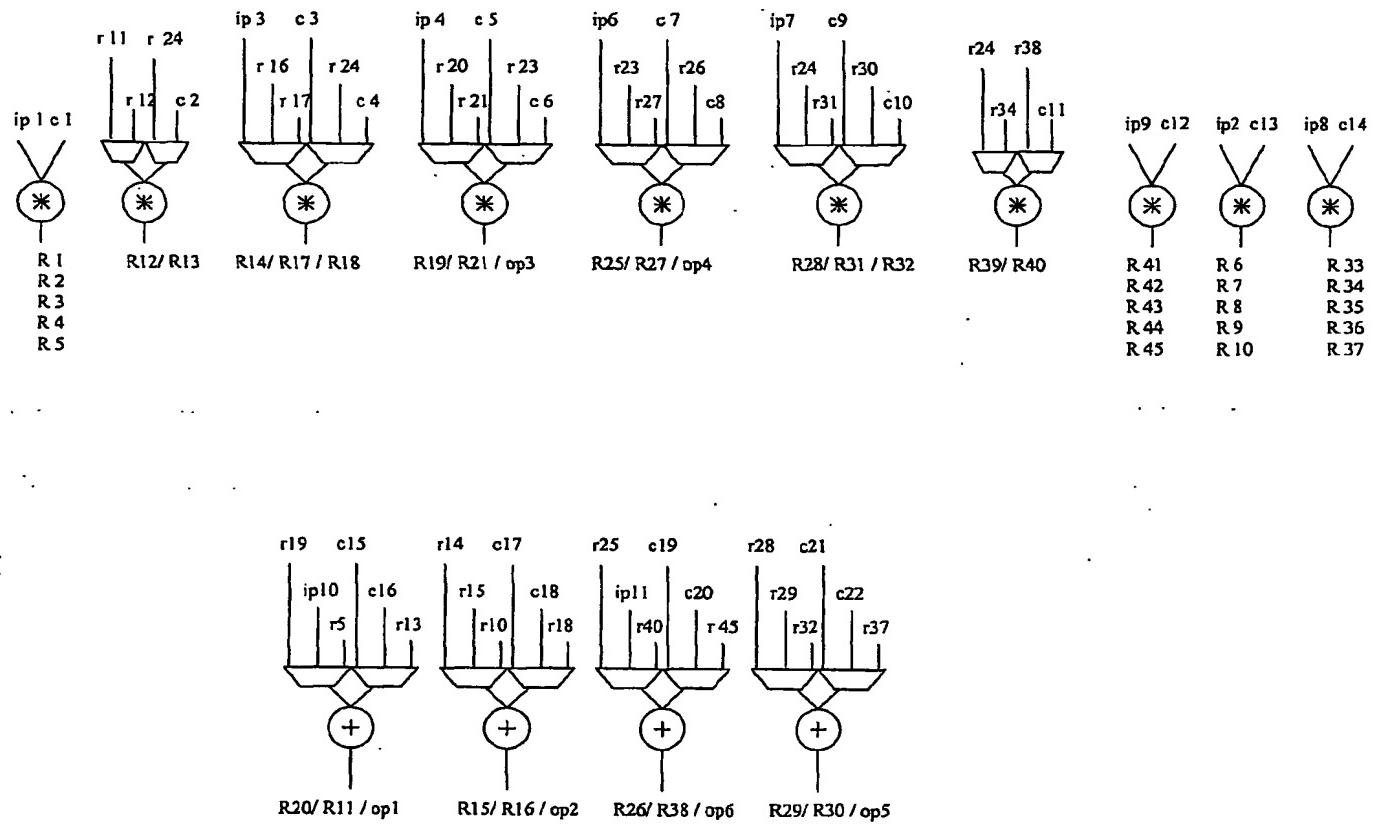


Fig:X Affine preloop common architecture after ASAP schedule

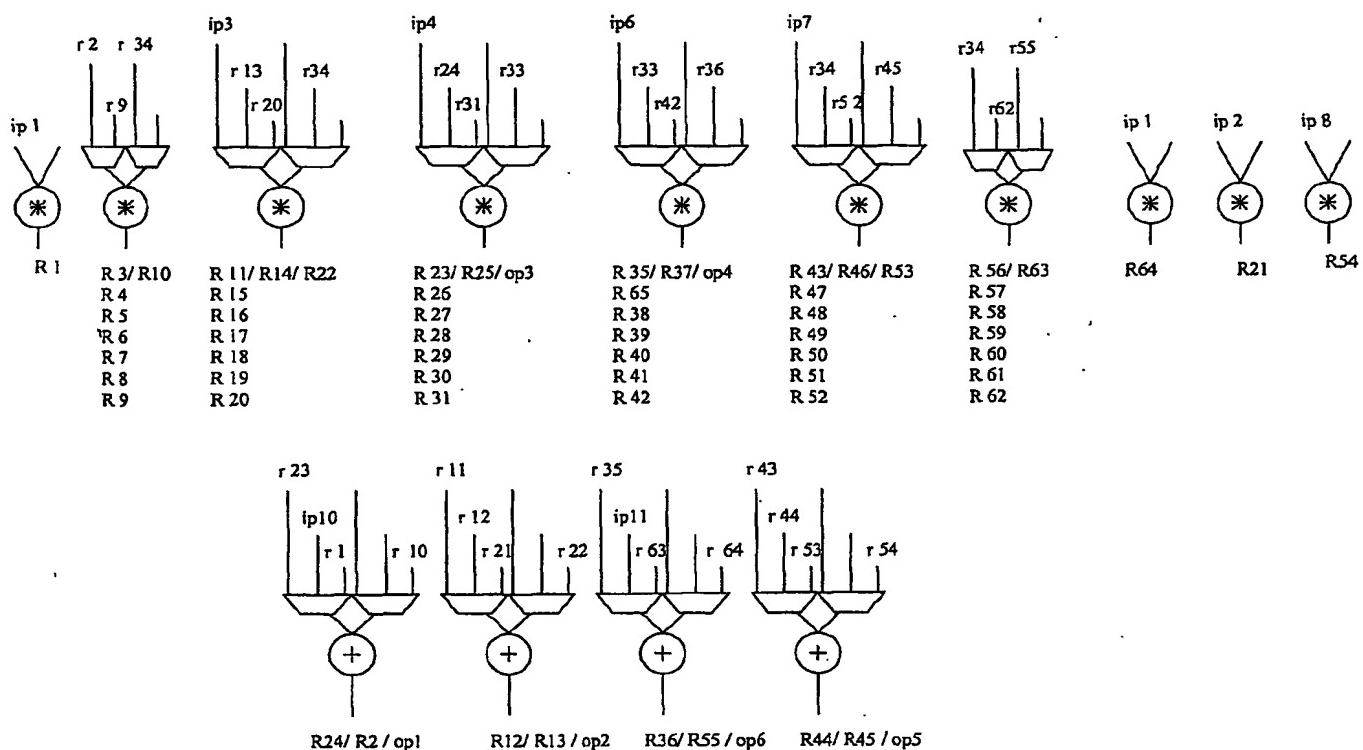
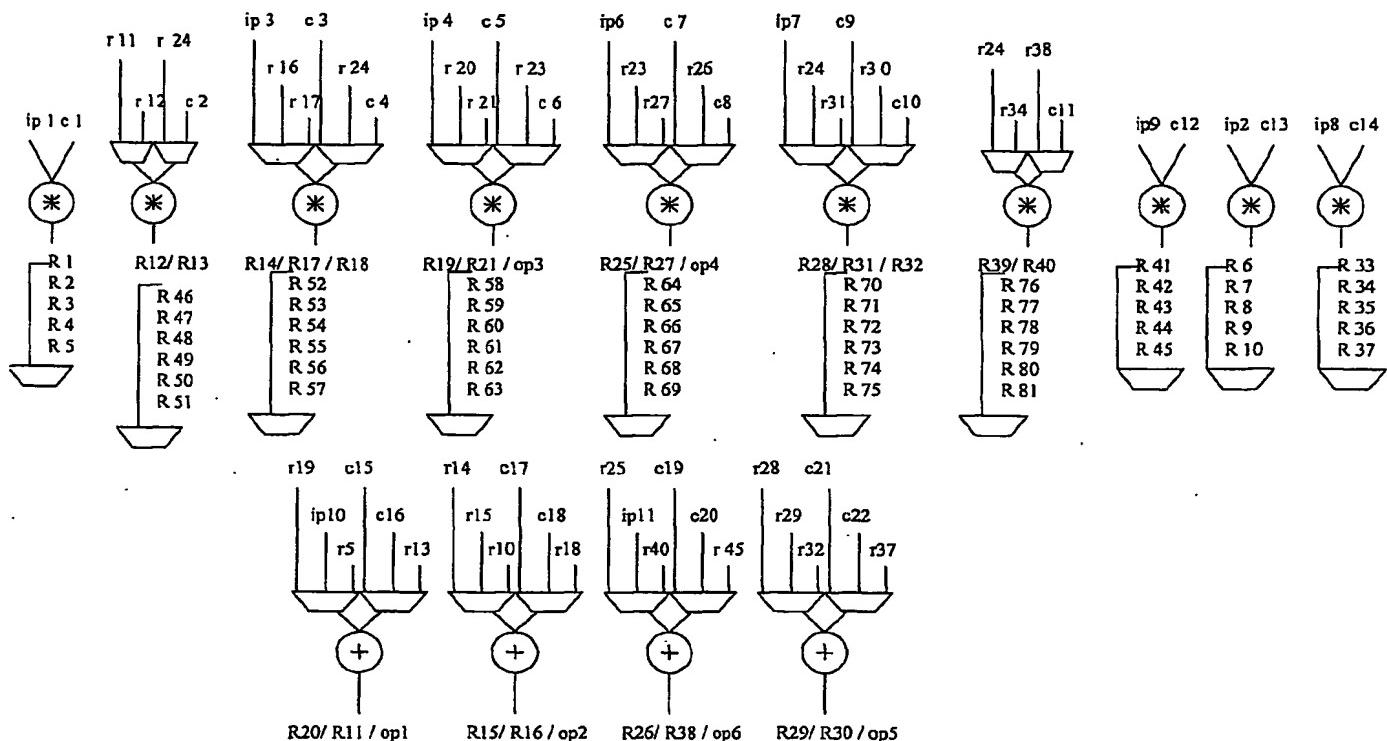


Figure 7: Perspective preloop common architecture after ASAP schedule



Note: Some multiplier and adder outputs also form outputs from the module.

Figure 2 Common architecture with multiplexers in delay paths to accommodate both affine and perspective instantiations.

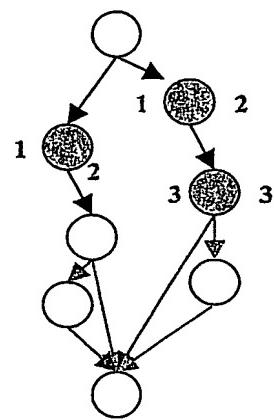
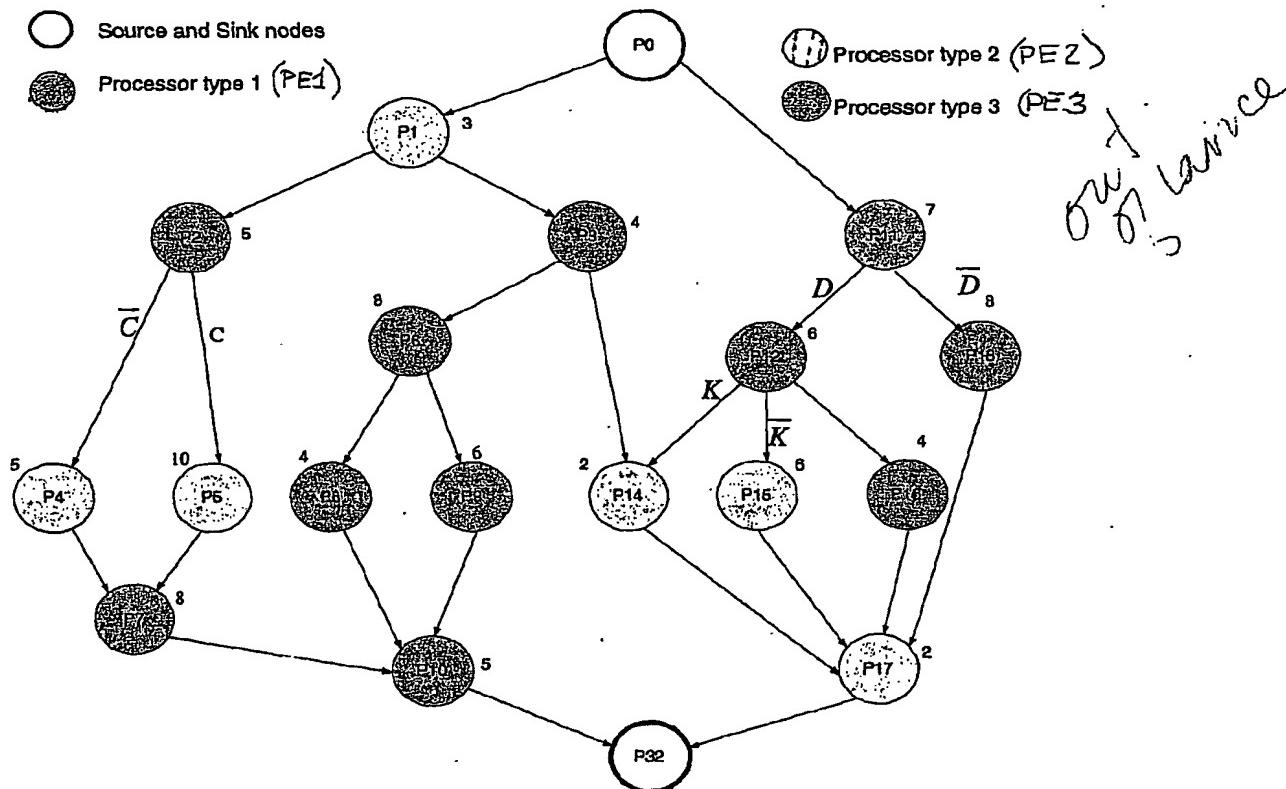


Figure 12: Path based edge activation

~~Illustrative example for our scheduling algorithm~~

(A) This example demonstrates ~~the~~ initialization strategy. It describes how the CDFG is split into individual DFGs. Moreover, it also shows the various fields required for each node and edge.

A. Initial CDFG:



For the CDFG of Fig. 13x

B. Initialization of CDFG data structure and Branching tree *proceeds as follows:*

Var_indices: var[0] = D; var[1] = C; var[2] = K;

Assume number of processing elements of type = 1

Branching tree paths: DCK, DCK', DC'K, DC'K', D'CK, D'CK', D'C'K, D'C'K'

Branching tree paths not possible: D'CK, D'CK', D'C'K, D'C'K'

Removing K we get: D'C, D'C'

Final Branching tree paths: DCK, DCK', DC'K, DC'K', D'C, D'C'.

Tables XX and YY are the node and edge lists, respectively, for the CDFG of Fig. 13x. Figs. 14x - 19x are the individual Data Flow Graphs (DFGs) of the CDFG of Fig. 13x.

C. List of individual DFGs:

DFG[0] → DCK

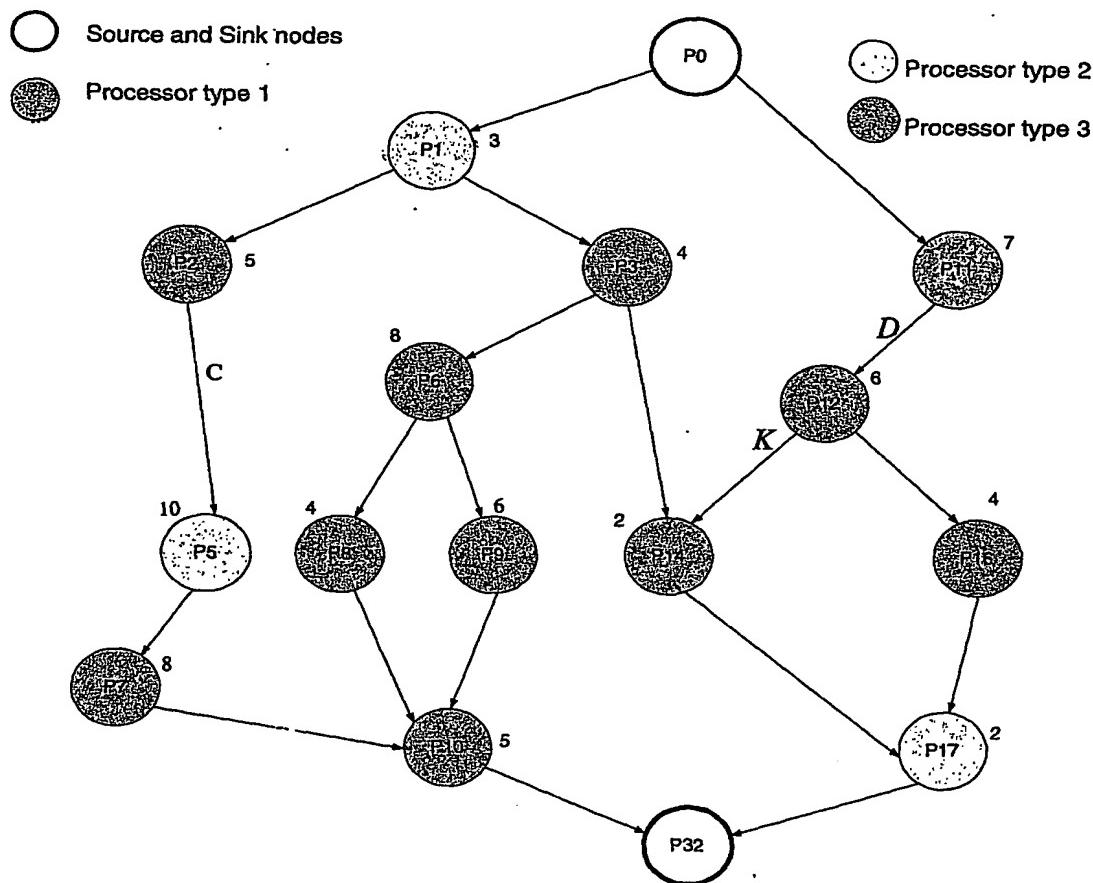


Fig 14x

DFG[1] → DCK'

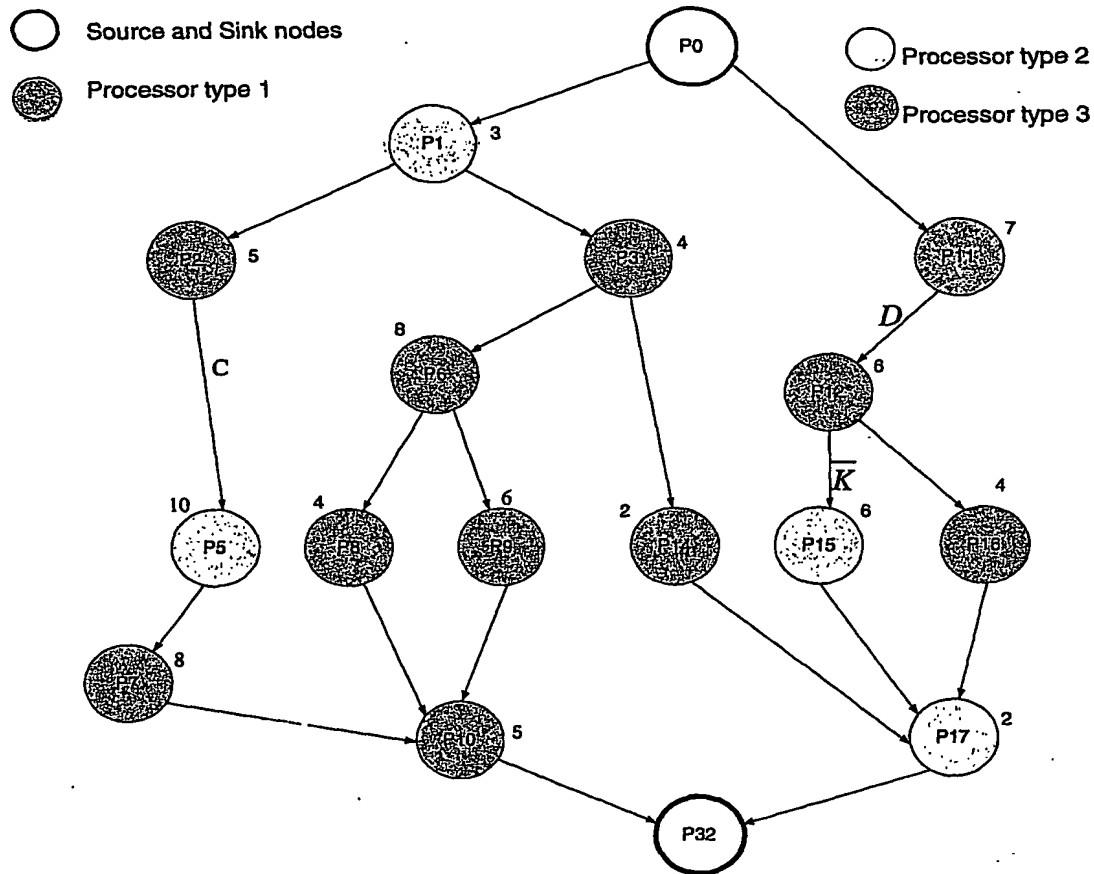


Fig. 15x

DFG[2] → DC'K

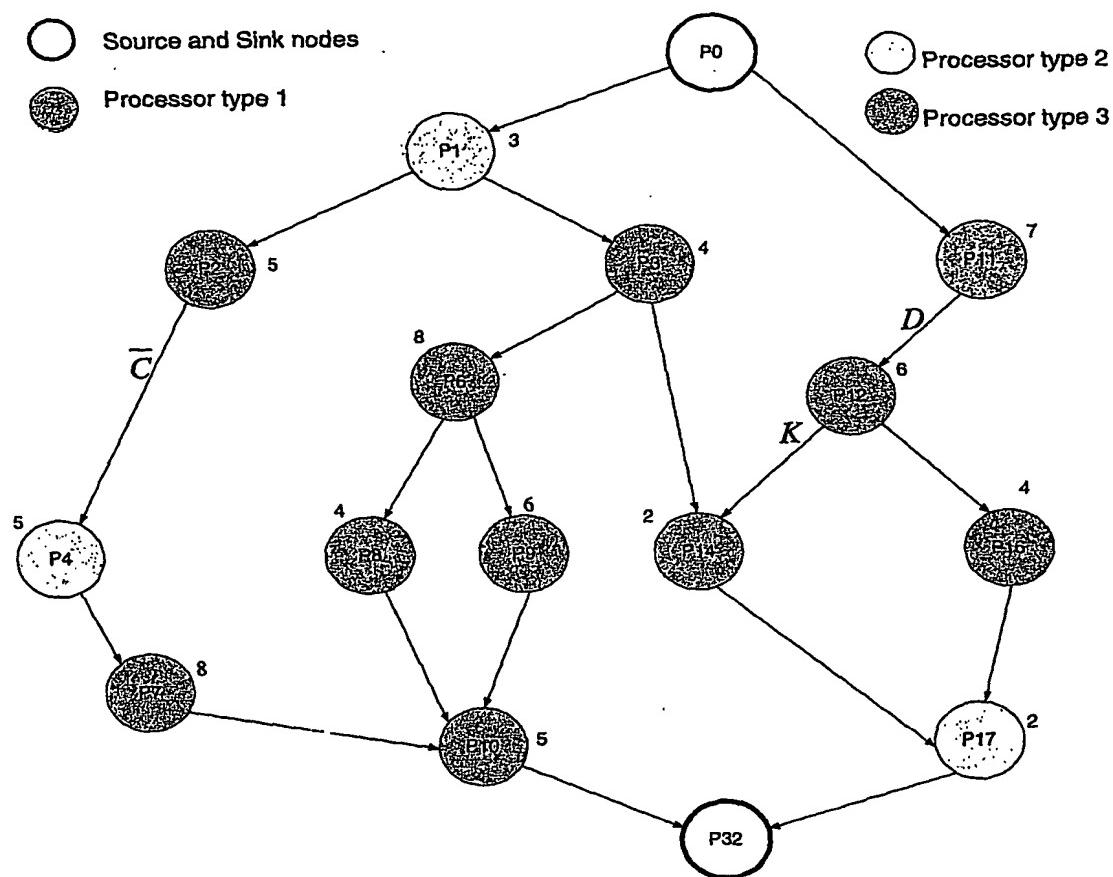


Fig. 16X

DFG[4] → D'C

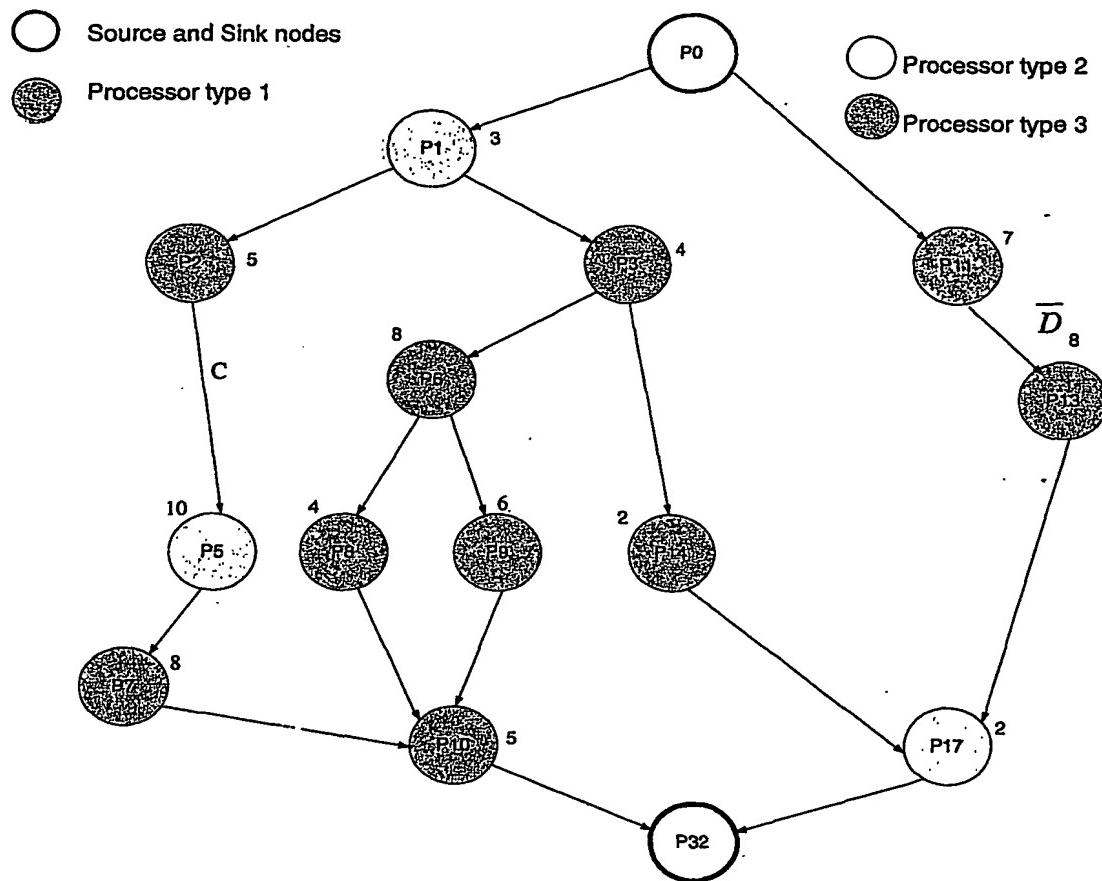


Fig 18x

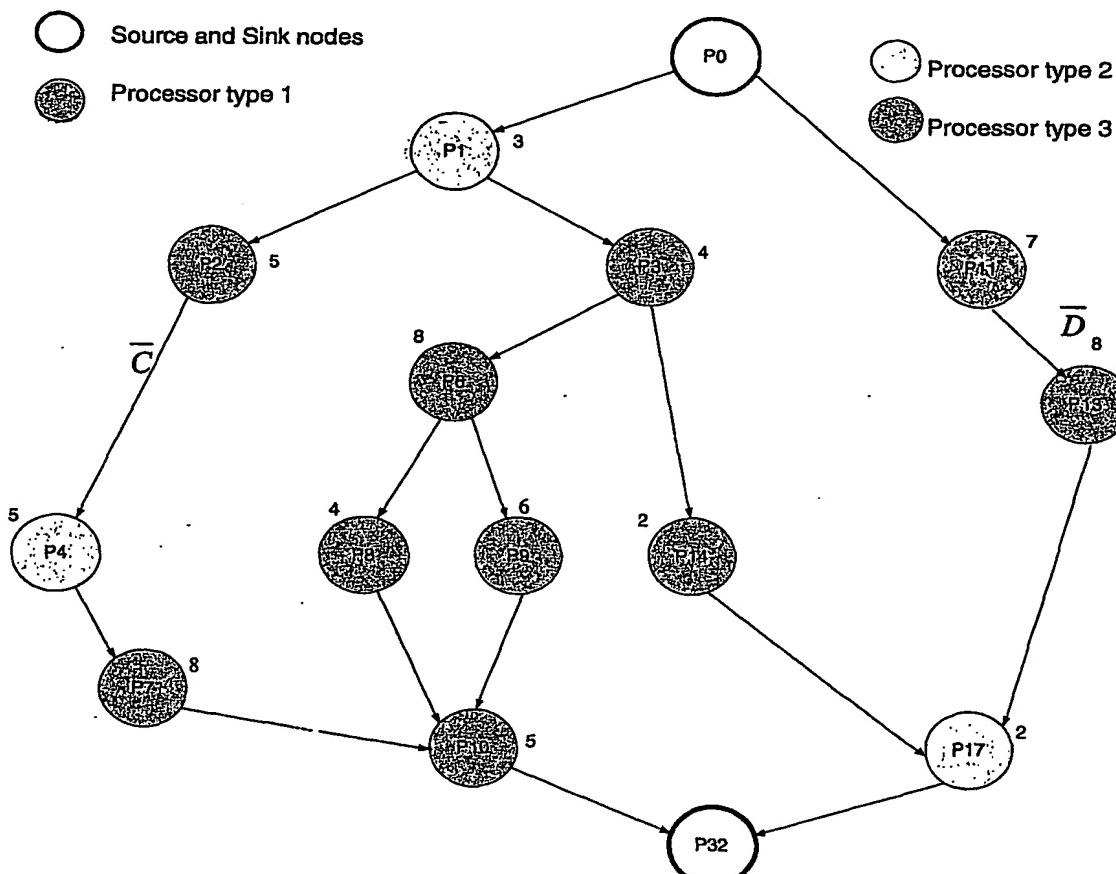
$DFG[5] \rightarrow D'C'$ 

Fig 19x

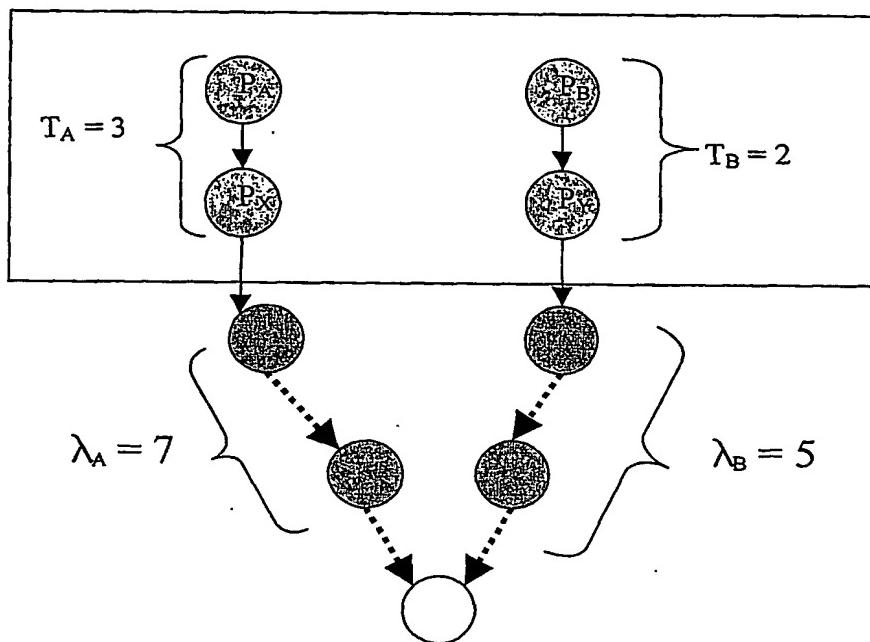
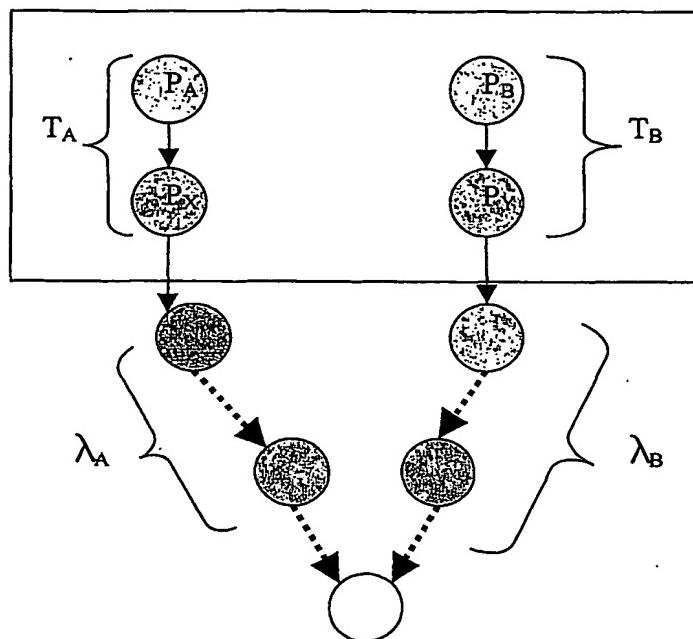
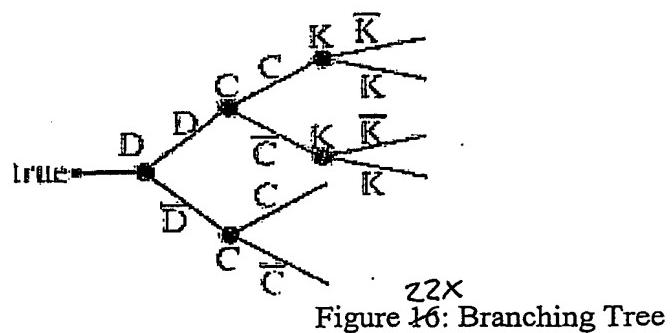
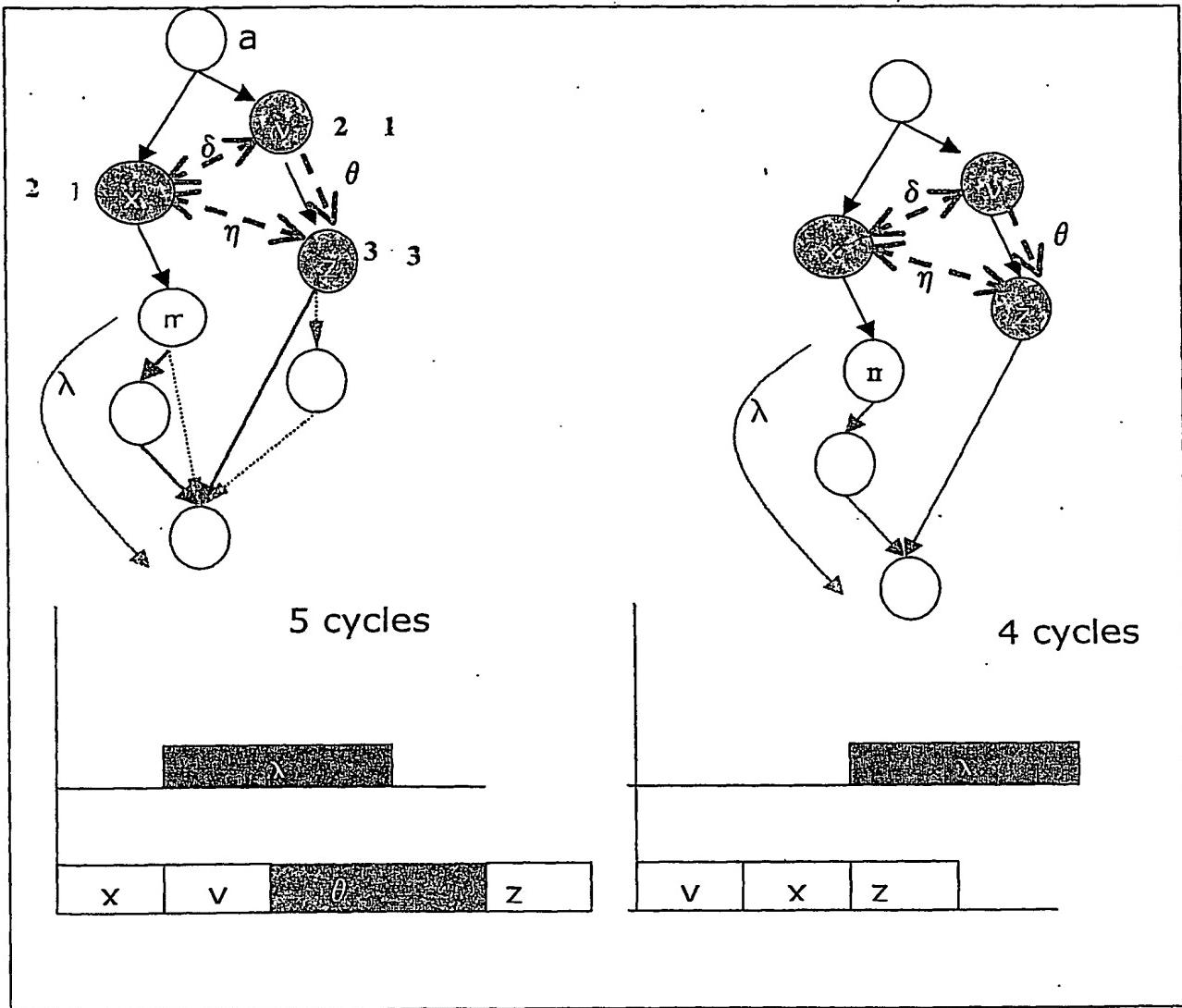


Figure 15: PCP Scheduling with Resource Dependencies in the Partial Path Region

2/1X
Figure 14: PCP based Scheduling2/2X
Figure 16: Branching Tree



23x
Figure 17: Influence of Reconfiguration time on Scheduling

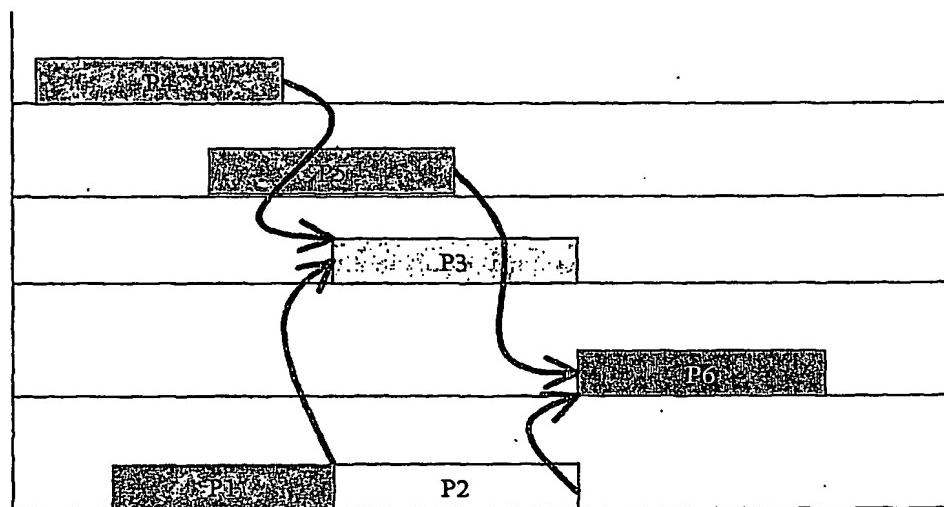


Figure 18: Scheduled Process Charts with Resource and Data Dependency
24X

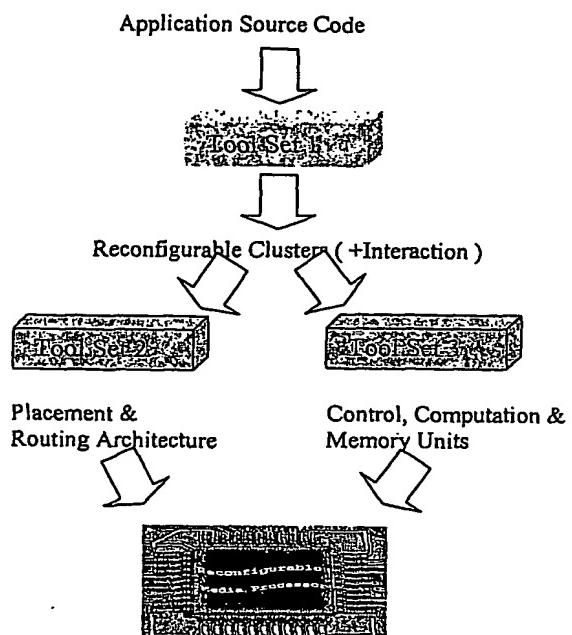
	Expression α	Expression β	Expression θ	Expression γ
Process A		0		
Process B		10		
.....				
.....				

	Expression α	Expression β	Expression θ	Expression γ
Process A		30		
Process B		40		
.....				
.....				

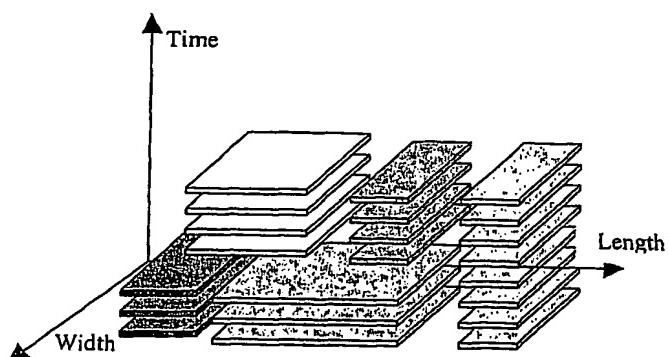
↓

and so on.

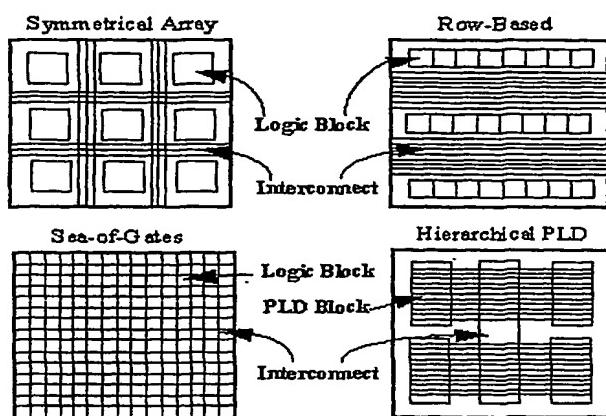
~~25X~~
Figure 19: Dynamic Entry Updates in the NSM and LSMS



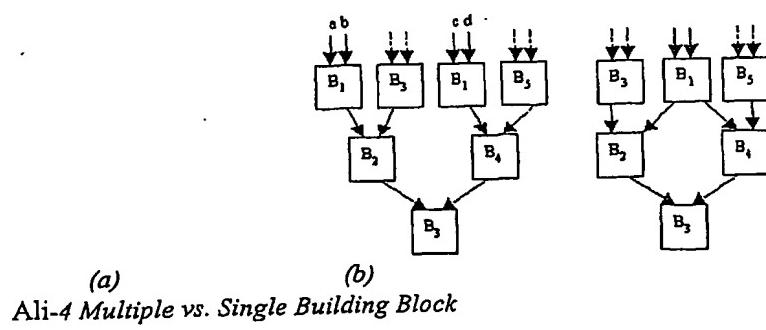
Ali-1 Tool Set Overview



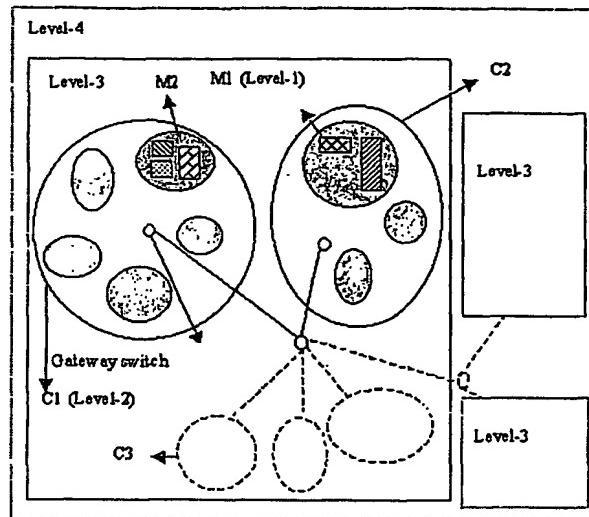
Ali-2 Constraints



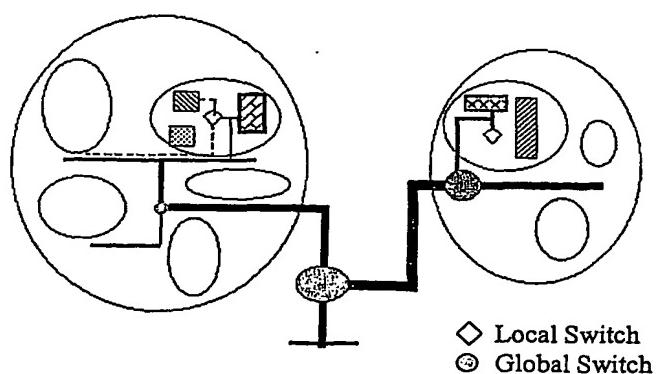
Ali-3 Routing Architecture Overview



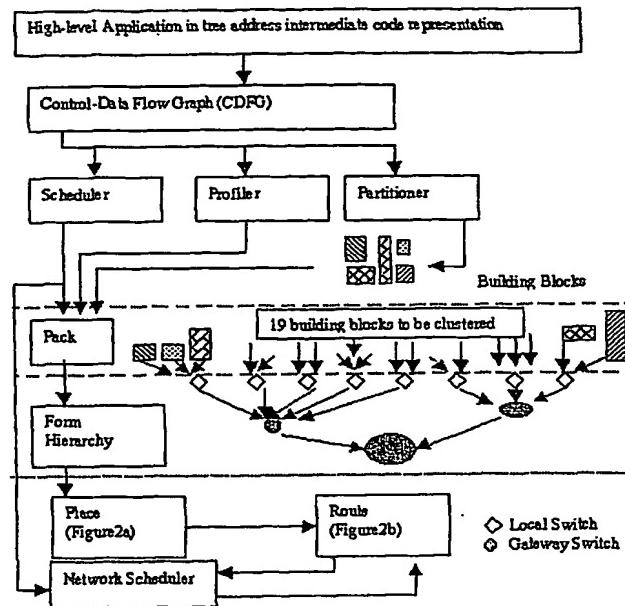
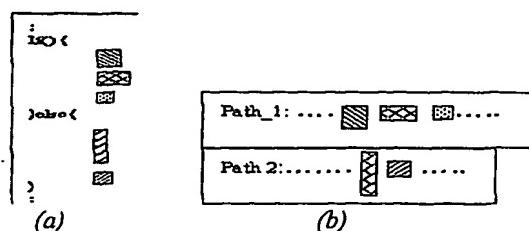
Ali-4 Multiple vs. Single Building Block



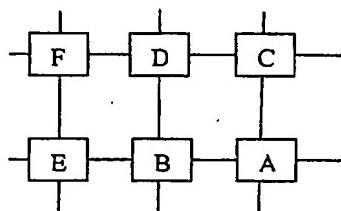
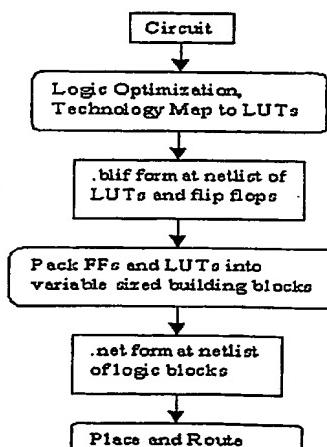
Ali-5 Overall Architecture

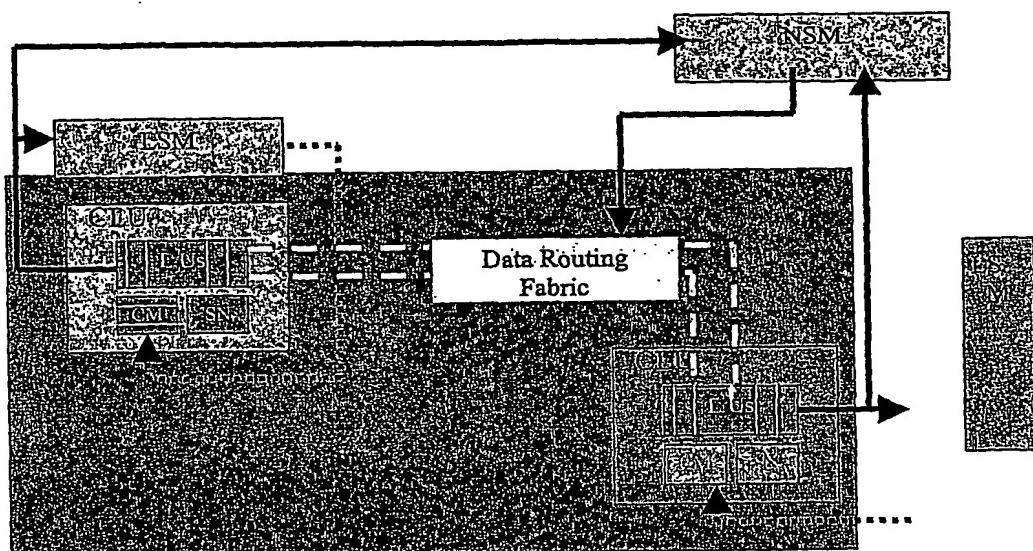


Ali-6 Switching

*Ali-7 Methodology**Ali-8 Control Flow Effect on Clusters*

	A	B	C	D	E	F
A	0	X	X	X	X	X
B	5	0	X	X	X	X
C	6	0	0	X	X	X
D	4	3	7	0	X	X
E	1	4	1	0	0	X
F	3	0	4	5	3	0

Ali-9a Cost matrix*Ali-9b Pre-placement**Ali-10 Design Flow*



CLU = Configurable Logic Unit; LU = Logic Units; SN = Switching Network
CM = Configuration Memory; LSM = Logic Schedule Manager

Figure 21: The Internals of the Reconfigurable Unit

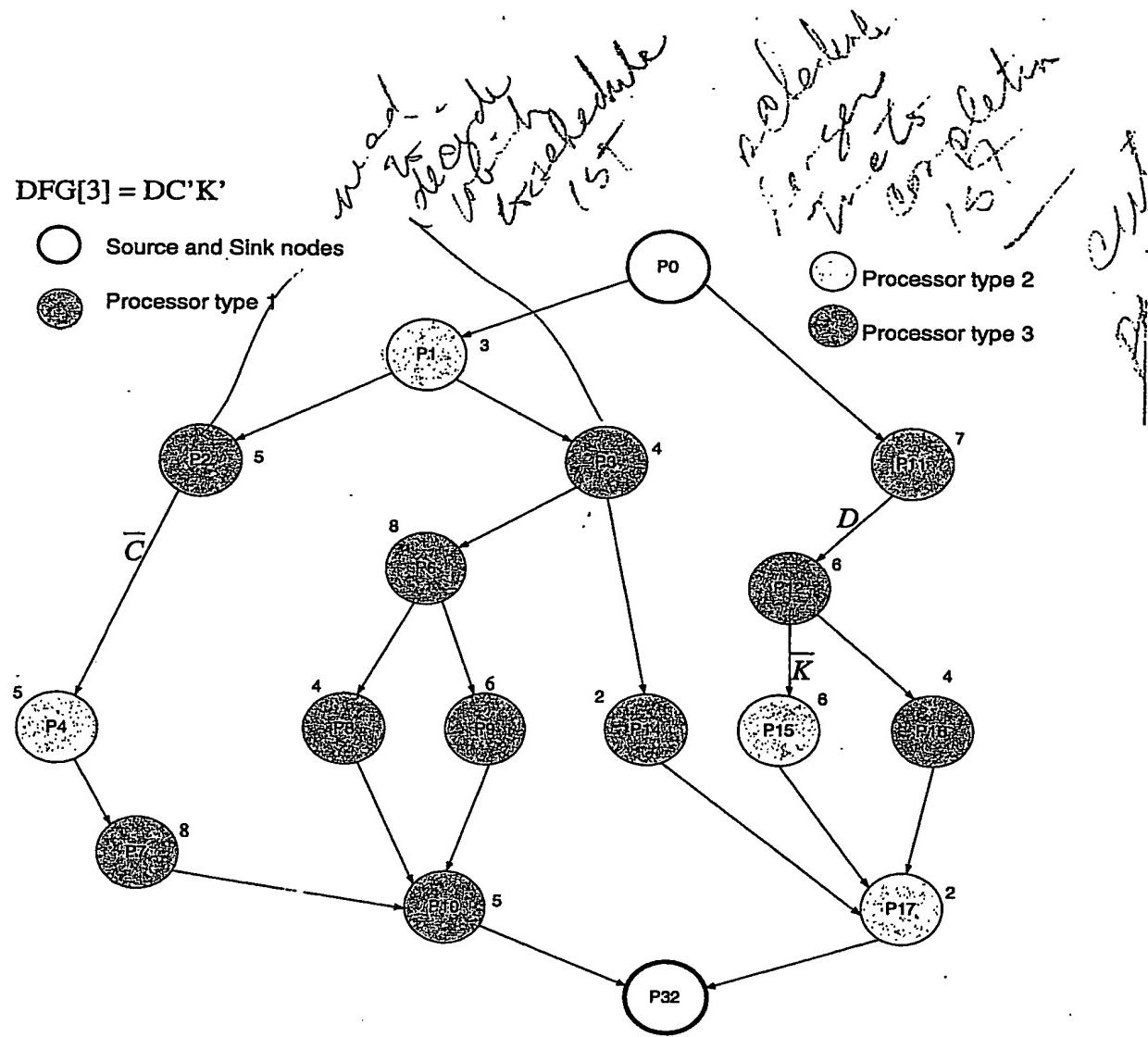


Fig 17x

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